Unit	Domain	Lab / Assignment	Lab / Assignment Topic	Exercise	Type	Hours	Recordings	Learning Outcome
Unit - 1	CMOS	Assignment - 1	CMOS Concepts	Understaing CMOS Concepts	Study assignment	40 Min	ALS/Lecture_1	L1
Unit - 1	CMOS	Lab_1 and Lab_2	HSPICE Simulations	IV Curves for PMOS & NMOS and assignments on HSPICE	Understand, apply and Analyse : Analytical Assignment	1.5 Hours	ALS/Lecture_2	L1
Unit - 2	Circuits	Lab_3	HSPICE Simulations + Layout Designing	Layout Designing for NAND and for boolean equtions	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lecture_3	L1
Unit - 2	Delays	Assignment - 2	Delay Estimation and Layout Comparision	Delay calculation using RC Delay Model and Elmore Delay	Study, Evaluate & Analyze	1 Hour	ALS/Lecture_4	L1
Unit - 2	Circuits	Assignment - 3	Timing in Sequential Circuits	Understanding timing issues in sequential circuits and solving the problems	Study, Evaluate & Analyze	1 Hour	ALS/Lecture_5	L1
Unit - 2	Delays	Assignment - 4	Logical effort and Design Optimization	Understanding Logical Effort	Study, Evaluate & Analyze	1 Hour	ALS/Lecture_6	L1
Unit - 2	Circuits	Lab_4 and Lab_5	HSPICE Simulations	Designing the circuit using Hspice	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lecture_7	L1
Unit - 3	Synthesis	Assignment - 5	Basic concepts of Synthesis	Understanding Synthesis Concepts	Study assignment	1 Hour	ALS/Lecture_8	L2
Unit - 3	Synthesis	Assignment - 6	Libraries	Understanding the .lib format and extracting characterstics of AND, OR amd D Flip Flop Families	Understand and Analyse	2 Hours	ALS/Lecture_9	L2
Unit - 3	Synthesis	Assignment - 7	Simulation and Synthesis mismatch	Writing efficient RTL to overcome simulation and synthesis mismatches	Understand, Evaluate and Analyse	1 Hour	ALS/Lecture_10	L2
Unit - 3	Synthesis	Assignment - 8	Library Setting and parsing the design	Invoking Design Compiler and Parsing the design	Understand and Analyse	1 Hour	ALS/Lecture_11	L2 + L3
Unit - 3	Synthesis	Assignment - 9	Environment Setup	Understanding the importance of PVT conditions, and Environment Setup	Understand and Analyse	1 Hour	ALS/Lecture_12	L2 + L3
Unit - 3	Synthesis	Assignmnt - 10	Design Constraints	Understanding the importance, types, priorities of design constraints	Understand and Analyse	1 Hour	ALS/Lecture_13	L2 + L3
Unit - 3	Synthesis	Assignment - 11	Compile flow and statergies	Understanding different types of Compile Statergies	Understand and Analyse	1 Hour	ALS/Lecture_14	L2 + L3
Unit - 3	Synthesis	Lab_6	Library Setting and parsing the design	Library Setup, understanding different DC commands, parsing(Analyze, Elobrate) the design, generating and analysing unmapped netlist	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lab_1	L2 + L3
Unit - 3	Synthesis		Defining the Constraints and Compiling the design	Checking the design, environment setup, Defining the constraints and compiling the design	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lab_2	L2 + L3
Unit - 3	Synthesis		Compiling and Analysis	Compiling and Analysis	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lab_3	L2 + L3
Unit - 3	Synthesis	Assignment - 12			Study & Analyze	1 Hour	ALS/Lecture_15	L2 + L3
Unit - 3	Synthesis		Analysis and Reporting	Analysis and Reporting		1 Hour 20 Min	ALS/Lab_4	L2 + L3
Unit - 4	Synthesis	Lab_7	Advanced Synthesis and Optimization - 1	Understanding and implementing: DC_Ultra, FSM Compiler, Critical path re-synthesis, Grouping and ungrouping, Data Path Optimization	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lecture_16	L2 + L4 + L5

Unit - 4	Synthesis	Lab_7	Advanced Synthesis and Optimization - 1	Understanding and Implementing: Datapath Extraction & Optimization, Sequential Phase Inversion, Register Re-timing, Slack Borrowing,	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lecture_17	L2 + L4 + L5
Unit - 4	Synthesis	Lab_8 and Lab_9			Understand, apply and Analyse : Analytical Assignment	1 Hour 40 Min	ALS/Lecture_18	L2 + L4 + L5
Unit - 4	Synthesis		Power Analysis	Power Analysis with Clock Gating and Saif		1 Hour	ALS/Lab_5	L2 + L4 + L5
Unit - 5	STA	Assignment - 13	Static Timing Analysis Concepts and flow	Understanding Static Timing Analysis Concepts and flow	Study, Research and Analyze	1 Hour 20 Min	ALS/Lecture_19	L2 + L6
Unit - 5	STA	Assignment - 14	Interconnects and delay calculation	Understanding Interconnects and delay calculation	Study, Research and Analyze	1 Hour	ALS/Lecture_20	L2 + L6
unit - 5	STA	Assignment - 15	Clocks and Exceptions	Understanding & Applying Clocks and Exceptions	Study, Apply and Analyze	1.5 Hour	ALS/Lecture_21	L2 + L6
Unit - 5	STA	Assignment - 16	Maximum Load	Specify 10fF maximum load for out1 output port Specify a maximum load equivalent to 5 times the capacitance of the "I" pin of the cell BUFFX7 for all outputs, except out1	Study, Apply and Analyze	1 Hour	ALS/Lecture_22	L2 + L6
Unit - 5	STA	Assignment - 17	Maximum Load		Study, Apply and Analyze	1 Hour	ALS/Lecture_23	L2 + L6
Unit - 5	STA	Assignment - 18	STA	Write a Prime Time script for divided and multiplied clock	Study, Apply and Analyze	1 Hour	ALS/Lecture_24	L2 + L6
-	STA	Assignment - 19	STA	Write a Prime Time Script to Edge Shift and Drive Strength Modelling	Study, Apply and Analyze	1 Hour 20 Min	ALS/Lecture_25	L7
Unit - 5	STA	Lab_10	Static Timing Analysis	Performing STA for Synthesized netlist	Understand, apply and Analyse : Analytical Assignment	1.5 Hour	ALS/Lab_6	L2 + L6
Unit - 5	STA		Static Timing Analysis	Performing STA for P&R netlist	Understand, apply and Analyse : Analytical Assignment	1.5 Hour	ALS/Lab_7	L2 + L6
Unit - 5	STA		What - If Analysis	Setup & Hold fixes, Manual Netlist Editing	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lab_8	L2 + L6
Unit - 4	Synthesis	Assignment - 20	Bottom - up Compile with Characterization	Compiling the design with bottom - top approach	Understand, apply and Analyse : Analytical Assignment	1 Hour	ALS/Lab_9	L2